AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): A delay locked loop (DLL) block to generate a delay locked clock signal by delaying an external clock signal in a semiconductor device, comprising:

a clock buffer to receive the external clock signal and an inverted signal of the external clock signal to generate a plurality of internal clock signals;

a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a plurality of divided signals, each having a predetermined pulse width adjusted by the control signal, and output a selected divided signal as the divided signal; and

a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal,

wherein the clock divider includes:

a first divider to receive the one of the internal clock signals to generate a first divided signal having a first pulse width and a first period;

a second divider to receive the first divided signal to generate a second divided signal having the first pulse width and a second period and a third divided signal having a second pulse width and the second period;

a selector to selectively output the second divided signal and the third divided signal according to the control signal; and

a third clock divider to receive an output of the selector to generate the divided signal..

Claim 2 (Previously Presented): The DLL block as recited in claim 1, wherein the DLL circuit includes:

a plurality of delay lines, each delay line having a plurality of unit delays, to delay the plurality of internal clock signals and the divided signal;

a delay model to delay an output of the plurality of delay lines for a predetermined delay time to generate a feedback signal;

a phase comparator to compare a phase of a reference clock signal generated by the clock divider with a phase of the feedback signal to generate a comparison signal, wherein the reference clock signal is an inverted version of the divided signal;

a shift controller to generate a shift right signal or a shift left signal according to the comparison signal; and

a shift register to adjust delay amount of the delay lines in response to the shift right signal or the shift left signal.

Claim 3 (Cancelled)

Claim 4 (Currently Amended): The DLL block as recited in ~~claim 3~~claim 1, wherein the first divider includes:

a 1st NAND gate to perform a NAND operation by receiving the one of the internal clock signals;

a 2nd NAND gate to perform a NAND operation by receiving the one of the internal clock signals;

a 1st inverter to invert one of the internal clock signals;

a 3rd NAND gate to perform a NAND operation by receiving an output signal of the 2nd NAND gate;

a 4th NAND gate, which is cross-coupled with the 3rd NAND gate, to output the first divided signal by performing a NAND operation for an output signal of the 1st NAND gate;

a 5th NAND gate to perform a NAND operation by receiving output signals of the 3rd NAND gate and the 1st inverter;

a 6th NAND gate to perform a NAND operation by receiving output signals of the 4th NAND gate and the 1st inverter;

a 7th NAND gate to perform a NAND operation by receiving an output signal of the 6th NAND gate and outputting an output signal to the 2nd NAND gate; and

a 8th NAND gate, which is cross-coupled with the 7th NAND gate, to perform a NAND operation by receiving an output signal of the 5th NAND gate and outputting an output signal to the 1st NAND gate.

Claim 5 (Previously Presented): The DLL block as recited in claim 4, wherein the second divider includes:

a 9th NAND gate to perform a NAND operation by receiving the first divided signal;

a 10th NAND gate to perform a NAND operation by receiving the first divided signal;

a 2nd inverter to invert the first divided signal;

a 11th NAND gate to perform a NAND operation by receiving an output signal of the 10th NAND gate;

a 12th NAND gate, which is cross-coupled with the 11th NAND gate, to output the second divided signal by performing a NAND operation for an output signal of the 9th NAND gate;

a 13th NAND gate to perform a NAND operation by receiving output signals of the 11th NAND gate and the 2nd inverter;

a 14th NAND gate to perform a NAND operation by receiving output signals of the 12th NAND gate and the 2nd inverter;

a 15th NAND gate to perform a NAND operation by receiving an output signal of the 14th NAND gate and outputting an output signal to the 10th NAND gate; and

a 16th NAND gate, which is cross-coupled with the 15th NAND gate, to perform a NAND operation by receiving an output signal of the 13th NAND gate and outputting an output signal to the 9th NAND gate.

Claim 6 (Currently Amended): The DLL block as recited in claim 3claim 1, wherein the selector includes:

a first pass gate to pass the second divided signal to the second clock divider when the control signal is in a first logic level; and

a second pass gate to pass the third divided signal to the second clock divider when the control signal is in a second logic level.

Claim 7 (Previously Presented): The DLL block as recited in claim 5, wherein the third divider includes:

a 17th NAND gate to perform a NAND operation by receiving an output signal of the selector;

a 18th NAND gate to perform a NAND operation by receiving the output signal of the selector;

a 3rd inverter to invert the output signal of the selector;

a 19th NAND gate to perform a NAND operation by receiving an output signal of the 18th NAND gate;

a 20th NAND gate, which is cross-coupled with the 19th NAND gate, to perform a NAND operation for an output signal of the 17th NAND gate;

a 21st NAND gate to perform a NAND operation by receiving output signals of the 19th NAND gate and the 3rd inverter;

a 22nd NAND gate to perform a NAND operation by receiving output signals of the 20th NAND gate and the 3rd inverter and outputting a reference signal;

a 23rd NAND gate to perform an NAND operation by receiving an output signal of the 22nd NAND gate and outputting an output signal to the 18th NAND gate; and

a 24th NAND gate, which is cross-coupled with the 23rd NAND gate, to perform a NAND operation by receiving an output signal of the 21st NAND gate and outputting an output signal to the 17th NAND gate.

Claims 8-14 (Canceled)